CLAIMS

1. A method for protecting an input buffer, comprising the operations of:

lowering a current from a p-supply to an input buffer when an input voltage to the input buffer is tolerant HIGH, wherein the p-supply is a voltage supplied to a p-channel transistor in the input buffer;

setting the p-supply to a particular voltage when the input voltage to the input buffer is tolerant HIGH, the particular voltage being at a specific value such that input transistors within the input buffer do not experience overstress voltages.

2. A method as recited in claim 1, wherein overstress voltages are voltages having values higher than an internal voltage of a Ring I/O wherein the input buffer is located.

3. A method as recited in claim 1, wherein p-supply is prevented from supplying current to the input buffer when an input voltage to the input buffer is tolerant HIGH.

4. A method as recited in claim 1, wherein the p-supply is controlled using a p-supply p-channel transistor.

5. A method as recited in claim 4, wherein the p-supply p-channel transistor turns OFF when the input to the input buffer is tolerant HIGH, and wherein the p-supply p-channel transistor turns ON when the input to the input buffer is LOW.

6. A method as recited in claim 1, wherein the p-supply voltage is set to an internal voltage of a Ring I/O when the input to the input buffer is LOW, and wherein the p-supply

voltage is set to the internal voltage of a Ring I/O - V_{Tn} when the input to the input buffer is the tolerant HIGH voltage.

7. A method as recited in claim 1, further comprising the operation of using a generator to design a the voltage tolerant input buffer.

8. A voltage tolerant circuit for protecting an input buffer, comprising:

an n-channel pass gate transistor having a first terminal coupled to a pad I/O, a second terminal coupled an input of an input buffer, and a gate coupled to an internal ring voltage (Ring V_{DD}); and

a p-supply p-channel transistor having a gate coupled to the pad I/O, a first terminal coupled to Ring V_{DD}, and a second terminal coupled to a p-supply of the input buffer, wherein the p-supply is a voltage supplied to a p-channel transistor in the input buffer.

9. A voltage tolerant circuit as recited in claim 8, further comprising a p-channel transistor having a first terminal coupled the pad I/O, a gate coupled to Ring V_{DD}, and a second terminal coupled to a first terminal of an n-channel transistor.

10. A voltage tolerant circuit as recited in claim 9, wherein the n-channel transistor further includes a gate coupled to Ring V_{DD} and a second terminal coupled to the p-supply of the input buffer.

11. A voltage tolerant circuit as recited in claim 8, wherein the input buffer is an inverter.

12. A voltage tolerant circuit as recited in claim 11, wherein the inverter includes a p-channel transistor having a first terminal coupled to the p-supply of the input buffer, a gate coupled to the input of the input buffer, and a second terminal coupled to an output of the input buffer.

13. A voltage tolerant circuit as recited in claim 12, wherein the inverter further includes an n-channel transistor having a first terminal coupled to the output of the input buffer, a gate coupled to the input of the input buffer, and a second terminal coupled to ground.

14. A voltage tolerant circuit as recited in claim 8, wherein the voltage tolerant I/O is designed using a generator.

15. A voltage tolerant architecture, comprising:

an input buffer having an input, an output, and a p-supply, wherein the p-supply is a voltage supplied to a p-channel transistor in the input buffer; and

a voltage tolerant I/O circuit having an n-channel pass gate transistor having a first terminal coupled to a pad I/O and a second terminal coupled an input of an input buffer, and a p-supply p-channel transistor having a gate coupled to the pad I/O, a first terminal coupled to Ring V_{DD}, and a second terminal coupled to the p-supply of the input buffer.

16. A voltage tolerant architecture as recited in claim 15, wherein the voltage tolerant I/O circuit further includes a p-channel transistor having a first terminal coupled the pad I/O, a gate coupled to Ring V_{DD}, and a second terminal coupled to a first terminal of an n-channel transistor.

17. A voltage tolerant architecture as recited in claim 16, wherein the n-channel transistor further includes a gate coupled to Ring V_{DD} and a second terminal coupled to the p-supply of the input buffer.

18. A voltage tolerant architecture as recited in claim 15, wherein the input buffer is an inverter.

19. A voltage tolerant architecture as recited in claim 18, wherein the inverter includes a p-channel transistor having a first terminal coupled to the p-supply of the input buffer, a gate coupled to the input of the input buffer, and a second terminal coupled to an output of the input buffer.

20. A voltage tolerant architecture as recited in claim 15, wherein the voltage tolerant I/O circuit is designed using a generator.